REMARKS

This amendment is resubmitted in response to a Notice of Non-Compliant Amendment mailed December 27, 2006 citing that in claim 2, line 11, the inserted word "shift" was not underscored and marked as added. This was due to a typographic error by applicant. After telephone conference with the Examiner Jesse Moll on January 5, 2007 it was agreed that the Amendment will be resubmitted after correction of the error.

The specification has been amended on page 6, to correct a typographical error in the first full paragraph. See page 6, lines 10-15 of the specification where it states, "However, when one of the expander cores 104, 106 is placed in bypass mode, it will function as a single bit shift register 208, 222, and dummy bits must be provided at the proper time in the sequence of bits to ensure that data is properly loaded into the expander core that is not in the bypass mode. For example, if the second core 106 is placed in bypass mode, an initial dummy bit must be supplied to expander core 106."

As amended the last line beginning at 14 should read "For example, if the second core 106 is placed in bypass mode, an initial dummy bit must be supplied to expander core 104." No new matter has been added.

The Examiner objected to Claim 2 stating that the limitation "having first and second expander cores" renders the claim unclear. Accordingly, the Applicant has accepted the Examiner's suggestion and the claim has been amended to read "having a first expander core and a second expander core."

The Examiner rejected claims 1-2 under 35 U.S.C. 102(b) as being anticipated by IEEE Standard Test Access port and Boundary-Scan Architecture. In response to the Examiner's rejection, claims 1-6 have been amended to more clearly recite the Applicant's invention.

Claim 1 has been amended to recite "receiving operational codes including a dummy bit from a host computer into a multi-bit shift register and a single bit shift register to the multiple core expander to put all but one core expander of said multiple core expander in bypass mode utilizing a single bit shift register." No new matter has been added. Support can be found in the specification on page 6, lines 4-20 and illustrated in the drawings on Figure 2. In addition claim 1 has been amended to recite as shown in Figure 2, a state machine, with 206 input lines to the multi-bit shift register 212,

the internal register 204, and an output through the multiplexer 214 to the J-TAG port 122. The state machine decodes the operational input codes core expander not placed in bypass mode and serially reads data from, and serially writes data to, at least one internal register. Support can be found in the specification on page 5, lines 26-31. Finally, the state machine inputting a control signal to a multiplexer to shift data to the output port of the core expander not placed in bypass mode to either a series connected core expander or back to the host computer. Support can be found in the specification on page 6, lines 25-30 and page 7, lines 1-2.

With respect to claim 2, it has also been amended to recite "receiving operational codes including a dummy bit from a host computer to said multiple core expander to put all but one core expander of said multiple core expander in bypass mode utilizing a single bit shift register." The IEEE Standard Test Access Port and Boundary-Scan Architecture recited by the Examiner discloses the basic architecture of a boundary-scan circuit but does not disclose the limitations added by the Applicant to the basic structure to achieve advantages proposed by the limitations added by the amended claims.

Therefore, in view of the foregoing, Applicant submits that claims 1-2 as amended are now in condition for allowance and such action is respectfully requested.

The Examiner rejected claims 1-6 under 35 U.S.C. 102(b) as being anticipated by CYGNAL (Programming FLASH through the JTAG Interface). In response to the Examiner's rejection claims 1-6 have been amended to more clearly recite the Applicant's invention. Claims 1-6 as amended all recite "receiving operational codes including a dummy bit from a host computer into a multi-bit shift register and a single bit shift register to put all but one core expander of said multiple core expander in bypass mode utilizing a single bit shift register." Referring to Figure 2, the input from the host computer is fed to both the multi-bit shift register 212 at the port 120 and single bit register 208. As recited in the specification on page 6, lines 20-24, "If expander core 104 is placed in bypass mode, the input signal from the input J-tag port 120 is applied to both the single bit shift register 208 and to the multi-bit shift register 212. However, state machine 206 generates a control signal 218 that is applied to multiplexer 214 to select input 220 to shift data out over the output 219 of multiplexer 214.

It is axiomatic that the standard for lack of novelty under 35 U.S.C. 102(b) is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all of the claim's essential elements. The excerpts that the examiner has cited from the IEEE reference and the Cygnal reference do not disclose Applicant's limitations as amended.

Although the Cygnal reference teaches the use of a state machine, the Applicant's limitation of receiving operational codes including a dummy bit from a host computer into a multi-bit shift register and a single bit shift register using a single bit register in combination with a state machine and multiplexer to place an expander in the output mode and shift data out is not taught by the Cygnal reference.

In view of the foregoing Applicant respectfully submits that claims 1-6 are now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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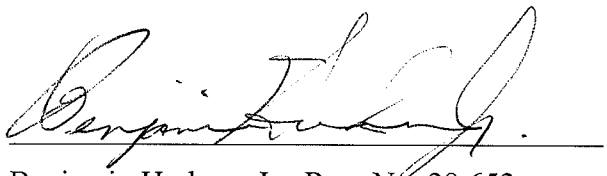

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